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DOCKET NO.: P05792
CLIENT NO.: NATI15-05792
Customer No.: 23990

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	RICHARD W. FOOTE ET AL.
U.S. Serial No.	:	10/777,012
Filed	:	February 11, 2004
For	:	SEMICONDUCTOR APPARATUS COMPRISING BIPOLAR TRANSISTORS AND METAL OXIDE SEMICONDUCTOR TRANSISTORS AND MANUFACTURING METHOD
Group No.	:	2632
Examiner	:	Not Yet Assigned

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

The undersigned hereby certifies that the following documents:

1. Postcard receipt;
2. Information Disclosure Statement;
3. Form PTO/SB/08A and PTO/SB/08B; and
4. Thirty-one (31) references.

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to, MAIL STOP AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 14, 2004.

Date: July 14, 2004

Kathleen Dunsmore
Mailer

Date: July 13, 2004

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Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents and publications herein are listed below and on the attached Forms PTO/SB/08A and PTO/SB/08B. Copy of the listed patents and publications are submitted herewith.

U.S. Patent No.	Inventor	Date
4,318,751	Horng	March 9, 1982
4,545,087	Nahum	October 8, 1985
4,922,318	Thomas et al.	May 1, 1990
5,037,768	Cosentino	August 6, 1991
5,104,816	Verret et al.	April 14, 1992
5,141,891	Arima et al.	August 25, 1992
5,294,558	Subbanna	March 15, 1994
6,472,324	Kusakabe et al.	October 29, 2002

Publications

M. Shimizu et al., "A Novel Polysilicon Source/Drain Transistor with Self-Aligned Silicidation", LSI R&D Laboratory, Mitsubishi Electric Corporation, Pp. 11-12.

S. Hsia et al., "Polysilicon Oxidation Self-Aligned MOS (POSA MOS) - A New Self-Aligned Double Source/Drain Ion Implantation Technique for VLSI", IEEE Electron Device Letters, Vol. EDL-3, No. 2, February 1982, Pp. 40-42.

Kamal Rajkanan et al., "A High-Performance BICMOS Technology with Double-Polysilicon Self-Aligned Bipolar Devices", IEEE Electron Device Letters, Vol. EDL-8, No. 11, November 1987, Pp. 509-511.

Tiao-Yuan Huang et al., "A MOS Transistor with Self-Aligned Polysilicon Source-Drain", IEEE Electron Device Letters, Vol. EDL-7, No. 5, May 1986, Pp. 314-316.

C. S. Oh et al., "A New MOSFET Structure with Self-Aligned Polysilicon Source and Drain Electrodes", IEEE Electron Device Letters, Vol. EDL-5, No. 10, October 1984, Pp. 400-402.

W. Josquin et al., "The Integration of Double-Polysilicon NPN Transistors in an Analog BiCMOS Process", Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988 Pp. 149-152.

Tunenori Yamauchi et al., "High Speed BICMOS Technology with Emitter-base Self-aligned Structure", Bipolar IC Division Fujitsu Limited, Pp. 155-158.

Kwang Soo Kim et al., Bipolar-Complementary-Metal-Oxide-Semiconductor (BiCMOS) Technology with Polysilicon Self-Aligned Bipolar Devices", Japanese Journal of Applied Physics, Vol. 30, No. 10, October 1991, Pp. 2459-2465.

Masahiro Shimizu et al., "A Novel CMOS Structure with Polysilicon Source/Drain (PSD) Transistors by Self-Aligned Silicidation", IEICE Trans. Electron, Vol. E76-C, No. 4, April 1993, Pp. 532-540.

M. K. Moravvej-Farshi et al., "Novel Self-Aligned Polysilicon-Gate MOSFETS with Polysilicon Source and Drain, Solid-State Electronics, Vol. 30, No. 10, 1987, Pp. 1053-1062.

W. R. Burger et al., "An Advanced Self-Aligned BiCMOS Technology for High Performance 1-MegaBit ECL I/O SRAM's", National Semiconductor Corp., Puyallup Technology Development, 1989.

James Warnock et al., "BiCMOS Technology with 60-Ghz n-p-n Bipolar and 0.25-μm CMOS", IEEE Electron Device Letters, Vol. 13, No. 11, November 1992, Pp. 578-580.

J. D. Hayden et al., "Integration of a Double Polysilicon, Fully Self-Aligned Bipolar Transistor into a 0.5μm BiCMOS Technology for Fast 4MBit SRAMs", Advanced Products Research and Development Laboratory, Motorola Inc., IEEE 1991 Bipolar Circuits and Technology Meeting, Pp. 17-20.

T. C. Mele et al., "A High Performance 0.5μm BiCMOS Triple Polysilicon Technology for 4mb Fast SRAMs", Advanced Products Research and Development Laboratory, Motorola Inc., IEEE 1990.

Kenneth O'Peter Garone et al., "A Double-Polysilicon Self-Aligned npn Bipolar Process (ADRF) with Optional NMOS Transistors for RF and Microwave Applications", 1994 Bipolar/BiCMOS Circuits & Technology Meeting, Pp. 221-224.

Alain Chantre et al., "Identification of a Corner Tunneling Current Component in Advanced CMOS-Compatible Bipolar Transistors", IEEE Transactions on Electron Devices, Vol. 38, No. 1, January 1991, Pp. 107-110.

K. Ishimaru et al., "Bipolar Installed CMOS Technology without Any Process Step Increase for High Speed Cache SRAM", IEEE 1995.

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Tzu-Yin Chin et al., "The Design and Characterization of Nonoverlapping Super Self-Aligned BiCMOS Technology", IEEE Transactions on Electron Devices, Vol. 38, No. 1, January 1991, Pp. 141-150.

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T. Yoshimura et al., "0.6 μm High Speed BiCMOS Technology with Emitter-Base Self-Aligned Structure", Fujitsu Limited, Bipolar IC Division, IEEE 1989, Pp. 241-244.

K. G. Moerschel et al., "Best: A BiCMOS-Compatible Super-Self-Aligned ECL Technology", AT&T Microelectronics, AT&T Bell Laboratories, IEEE 1990 Custom Integrated Circuits Conference, Pp. 18.3.1-18.3.4.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

Respectfully submitted,

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Date: July 13, 2004

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 4

Complete if Known	
Application Number	10/777,012
Filing Date	02/11/2004
First Named Inventor	Richard W. Foote
Art Unit	2632
Examiner Name	Not Yet Assigned
Attorney Docket Number	P05792

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	US- 4,318,751	03/09/1982	Horng	
	AB	US- 4,545,087	10/08/1985	Nahum	
	AC	US- 4,922,318	05/01/1990	Thomas et al.	
	AD	US- 5,037,768	08/06/1991	Cosentino	
	AE	US- 5,104,816	04/14/1992	Verret et al.	
	AF	US- 5,141,891	08/25/1992	Arima et al.	
	AG	US- 5,294,558	03/15/1994	Subbanna	
	AH	US- 6,472,324	10/29/2002	Kusakabe et al.	
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Examiner Signature		Date Considered	

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NON PATENT LITERATURE DOCUMENTS

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	BA	M. Shimizu et al., "A Novel Polysilicon Source/Drain Transistor with Self-Aligned Silicidation", LSI R&D Laboratory, Mitsubishi Electric Corporation, Pp. 11-12.	
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	CJ	Tadanori Yamaguchi et al., "Process Integration and Device Performance of a Submicrometer BiCMOS with 16-Ghz ft Double Poly-Bipolar Devices", IEEE Transactions on Electron Devices, Vol. 36, No. 5, May 1989, Pp. 890-896.	

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